A/D Converters for Wireless Communication in Nanometer CMOS

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Introduction
Evolution of RF Transceivers

- CMOS Technology scaling – Moore’s law
- Circuit design technique innovations

Past

Ericsson CH388 (Hybrid, 1995)

Ericsson Bluetooth (CMOS, 2001)

Berkanå GSM/GPRS (CMOS, 2005)

Present

Radio

Future

Nano-CMOS?

Nanotube?
A/D Interface in RF Receivers

1. RF Filter → RF-FE → AAF → SCF, GmC OP-RC → A/D → DSP
   - Analog CSF

2. RF Filter → RF-FE → AAF → A/D → DSP
   - Digital CSF

3. RF Filter → LNA → A/D → Dig. Mod. → Dig. Filter → DSP
   - SDR

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Example: GSM Receiver

<table>
<thead>
<tr>
<th>Specs</th>
<th>Case 1 (Analog CSF)</th>
<th>Case 2 (Digital CSF)</th>
<th>Case 3 (SDR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic Range</td>
<td>20-40 dB</td>
<td>60-80 dB</td>
<td>100 dB</td>
</tr>
<tr>
<td>Sample Rate</td>
<td>0.4 MHz</td>
<td>1.6 MHz or 2*IF</td>
<td>2 GHz</td>
</tr>
<tr>
<td>Architecture</td>
<td>Nyquist</td>
<td>Sigma-Delta</td>
<td>?</td>
</tr>
<tr>
<td>Power</td>
<td>1 mW</td>
<td>10 mW</td>
<td>?</td>
</tr>
</tbody>
</table>

Trivial Doable Outrageous!

- Fundamental tradeoff between linearity (DR) and power consumption
- Judicial system partition results in lowest cost (power, area, technology)
- Power efficiency and linearity are the key concerns for mobile txers
A/D Converter Basics
Signal Quantization

\[ D_{out} = 2^N \cdot \frac{V_{in}}{V_{FS}} \]

- Quantization = division + normalization + truncation
- Full-scale range \( (V_{FS}) \) is determined by \( V_{ref} \)

Static performance metrics:
- Monotonicity
- Differential nonlinearity (DNL)
- Integral nonlinearity (INL)
- Offset
- Gain error

Dynamic performance metrics:
- Signal-to-noise ratio (SNR)
- Signal-to-noise plus distortion ratio (SNDR)
- Spurious-free dynamic range (SFDR)
- Aperture uncertainty
- Dynamic range (DR)
- Idle channel noise (ΣΔ)
Quantization Error

\[
N = 3
\]

\[D_{\text{out}} \Delta - V_{\text{in}} = D_{\text{out}} \left( \frac{V_{FS}}{2^N} \right) - V_{\text{in}}\]

"Random" quantization error is regarded as noise

\[
\frac{-\Delta}{2} \leq \epsilon \leq \frac{\Delta}{2}
\]

\[
\sigma_{\epsilon}^2 = \int_{-\Delta/2}^{\Delta/2} \epsilon^2 \cdot \frac{1}{\Delta} \cdot d\epsilon = \frac{\Delta^2}{12}
\]

Assumptions:
- \( N \) is large
- \( 0 \leq V_{\text{in}} \leq V_{FS} \) and \( V_{\text{in}} \gg \Delta \)
- \( V_{\text{in}} \) is active
- \( \epsilon \) is Uniformly distributed
- Spectrum of \( \epsilon \) is white
SQNR, ENOB, and QN Spectrum

Assume $V_{in}$ is sinusoidal with $V_{p-p} = V_{FS}$

$$\text{SQNR} = \frac{V_{FS}^2}{\sigma_{\epsilon}^2} = \frac{(2^N \Delta)^2}{12} = 1.5 \times 2^{2N}$$

$$\text{SQNR} = 6.02N + 1.76 \text{dB}$$

$$\text{ENOB} = \frac{\text{SQNR} - 1.76}{6.02}$$

- SQNR depicts the theoretical performance of an ideal ADC
- In reality, ADC performance is limited by many other factors
  - Electronic noise (thermal, $1/f$, coupling, and etc.)
  - Distortion (measured by THD, SFDR)
Typical Nyquist ADC Output Spectrum

- Signal-to-noise plus distortion ratio (SNDR)
- Total harmonic distortion (THD)
- Spurious-free dynamic range (SFDR)

SNDR = 59.2 dB
ENOB = 9.54 bits
THD = 63.1 dB
SFDR = 64.0 dB

ENOB = \frac{SNDR - 1.76}{6.02}

- High-order harmonics are aliased back, visible in [0, \( f_s/2 \)] band
- Eg: HD3 @ 779x3+1=2338, HD9 @ 8192-9x779+1=1182
ADC Dynamic Performance

- Peak SNDR limited by large-signal distortion of the converter
- Dynamic range implies the “theoretical” SNR of the converter

\[
\text{SNDR} = 10 \log \left( \frac{V_{in}^2/2}{\Delta^2/12 + \sigma_N^2} \right)
\]

\[
\propto 20 \log(V_{in})
\]

\[
\propto V_{in} (\text{dB})
\]

- Circuit noise
- Overload
- Peak SNDR
- Dynamic range

[Diagram showing SNDR vs. Vin with graphical representation of contributions like Circuit noise and Overload.]
Sigma-Delta vs. Nyquist ADCs
Nyquist-Rate ADC

Architecture:
- Word-at-a-time (1 step)
  - Flash
  - Folding
- Level-at-a-time ($2^N$ steps)
  - Integration (Serial)
- Bit-at-a-time (N steps)
  - Successive approximation
  - Algorithmic (Cyclic)
- Partial word-at-a-time
  (1<$M$≤N steps)
  - Subranging
  - Multi-step
  - Pipeline

† Latency, not throughput

Sample by sample
Memoryless
Minimum sample rate

Nyquist-sampling
Sigma-Delta (ΣΔ) ADC

Nyquist-sampling

- Oversampling with $M \gg 1$
- Quantization noise shaping
- Low-resolution quantization
- Digital decimation filter required

Oversampling: much relaxed AAF

Noise PSD

Digital input $v_{\text{ref}}$ to $\Sigma\Delta$ mod, yielding digital output $d_1$. Decimation filter with OSR gives output $b_n$.

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Noise Shaping Basics

Push noise out of signal band

High gain @ LF, low gain @ HF
→ Integrator?
**ΣΔ Modulator**

1st-order ΣΔ modulator

- Integrator performs noise shaping
- D/A feedback to avoid ∫ saturation

Linearized z-domain model:

\[ Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z) \]

Signal Transfer Function:

\[ \text{STF} = z^{-1} \text{ ← Delay} \]

Noise Transfer Function:

\[ \text{NTF} = 1 - z^{-1} \text{ ← HP} \]
Noise Transfer Function

In-band quantization noise:

\[ N_e^2 \approx \frac{\Delta^2}{12} \cdot \frac{\pi^2}{3M^3} \]

\[ Y(z) = z^{-n}X(z) + (1 - z^{-1})^L E(z) \]

- Doubling OSR (M) increases SQNR by (6L+3) dB, or (L+0.5) bit
- Potential instability for 3rd- and higher-order single-loop \( \Sigma \Delta \) modulators
**ΣΔ vs. Nyquist ADCs**

**ΣΔ ADC output (1-bit)**

**Nyquist ADC output**

**Nyquist:**
- Sample by sample, memoryless, each sample resolved to N bits

**ΣΔ:**
- The digital codes only display an “average” impression of the input
- INL, DNL, monotonicity, missing code, and etc. do not directly apply in ΣΔ converters → use SNR, SNDR, SFDR instead (DR not rec’d)
Implementation Aspects of ΣΔ ADCs
Implementation Simplicity

- SC integrator, sampling at input
- 1-bit ADC → simple, ZX detector
- 1-bit feedback DAC → simple, inherently linear
- Quantization noise highly correlated with input → “tones”
Insensitive to Component Mismatch

\[
D_o(z) = \frac{\alpha}{z^2 + \alpha - 1} V_i(z) + \frac{(z - 1)^2}{z^2 + \alpha - 1} E(z)
\]

- Less correlation b/t \( E(z) \) and \( V_i(z) \)
- Simple, stable, highly-linear
- **Insensitive to component mismatch**
- Relaxed op-amp gain requirement
High-Order Single-loop ΣΔ Modulator

- Higher order noise shaping ($L \geq 3$) is obtained
- Relaxed circuit components w/ single-bit quantizer and D/A
- Subject to stability issues for $L \geq 3$
- Integrator gains and feedback coefficients need to be carefully optimized to avoid overload; resets each integrator output if occurs
Feedforward Compensation (1)

Eliminates circulating signal in the loop → less likely to be unstable
Only quantization noise processed by the integrators
Less signal swing at integrator outputs → less op-amp swing required and less distortion → good for low $V_{DD}$ implementation
Feedforward Compensation (2)

MATLAB simulations w/ nonlinear function included in 1st integrator

w/o feedforward†

w/ feedforward†

† Courtesy of Prof. Gabor Temes, OSU
The Cascaded Architecture (MASH)

- Idea: to further quantize $E(z)$ and later subtracted in digital domain
- The basic modulator is limited to $2^{nd}$ order → not subject to instability
- The $2^{nd}$ quantizer is typically a $\Sigma\Delta$ modulator as well
MASH 2-1 Cascaded Modulator

\[ Y(z) = z^{-3}X(z) - (1 - z^{-1})^3 E_2(z) \]

- \( E_1(z) \) completely cancelled assuming perfect matching between the modulator NTF (analog domain) and the DNTF (digital domain)
- A 3rd-order noise shaping on \( E_2(z) \) obtained w/o stability issues
- Caveat: sensitive to mismatch (analog NTF \( \neq \) digital NTF)
Integrator “Leakage”

$$H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}}, \quad \alpha < 1$$

- Finite op-amp gain introduces noise leakage into the signal band
- Leakage can also result in “dead zone” for small input voltages
How Much Gain Is Enough?

Set \( A_{\text{BLUE}} = N_e^2 \) (3dB loss in SQNR)

\[
A = \frac{M}{\pi^{\frac{2L+1}{2}}} \approx \frac{M}{\pi}
\]

- Input-referred circuit noise of the 1st integrator dominates over QN
- Actual required op-amp gain is determined by distortion specs
**DAC Nonlinearity**

2\textsuperscript{nd}-order $\Sigma\Delta$ Modulator (4-b A/D and D/A), OSR = 32, ideal SNDR $\approx$ 14 b

- **Ideal DAC†**
  - SNDR = 84.3 dB

- **10-bit linear DAC†**
  - SNDR = 60.5 dB

- 2-level SE or 3-level DF DAC can be made perfectly linear
- Multi-bit DAC nonlinearity directly adds to the summing node, limiting the $\Sigma\Delta$ Modulator linearity and quantization noise performance
- In general, linearity of $\Sigma\Delta$ Modulator is no better than that of the DAC – use mismatch-shaping DAC or DEM/DWA

† Courtesy of Prof. Gabor Temes, OSU
Integrator Noise and Distortion

\[
Y = X + N_1 + (1 - z^{-1})N_2 + (1 - z^{-1})^2N_3 + \delta(1 - z^{-1})^2E_1 + (1 - z^{-1})^3E_2
\]

INT1 dominates the overall noise and distortion performance!
Technology Scaling and Impact on $\Sigma\Delta$ ADC
"The number of transistors on a chip doubles every 18 months…"
- Gordon Moore, IEDM 1975

Source: www.intel.com
\( \Sigma \Delta \) ADC Design in nm-CMOS

Technology scaling offers:
- High \( f_T \)
- Low \( V_{DD} \)
- Elevated device noise
- Low intrinsic gain (\( g_m \cdot r_{out} \))
- Sub-threshold/gate leakage
- Better matching [Pelgrom98]

\( \Sigma \Delta \) ADC Design perspective:
- Faster amplifier \( \rightarrow \) large M
- Difficult to achieve high ENOB \( \rightarrow \) high power?
- High-gain amplifier?
- Switched-capacitor?
- Determined by size

- Large OSR enables wideband applications
- Noise shaping helps to reduce later stage power/area
- Decimation filter, DWA, digital correction/calibration scale well
ADC FoM Scaling (≥12 bits)

ΣΔ ADCs scale better than Nyquist ADCs!

FoM = \( \frac{\text{Power}}{2^{\text{ENOB}} \cdot f} \)  
\[ \text{Joule} \]  
\[ \text{Conversion Step} \]

Supply Voltage [V]

FoM [pJ/conv. step]

Sources: JSSC, ISSCC, CICC, VLSI, ESSCIRC

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CT ΣΔ ADC for Wireless Communication

- Integrator is replaced by CT resonator (also functions as AAF)
- Sampling is performed within the loop, not at very input
- Comparator and DAC (switched current) still work in discrete time
- Viable alternative to SC in nm-CMOS with leaky switches

LC, GmC, OP-RC

\[ V_i(s) \rightarrow H(s) \rightarrow D_0(z) \]

Resonator:

\[
H(s) = \frac{\omega_0 s}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}
\]
Challenges for CT $\Sigma\Delta$ ADC

- Large op-amp gain and BW required to make summing node ideal
- Integration is performed over the entire clock period of DAC – needs return-to-zero (RZ) pulse shaping to maintain constant pulse width
- Sensitive to DAC clock jitter – use multi-bit A/D, alternative D/A pulse
- Typically requires frequency tuning on $H(s)$ which is analog
Summary

• ADC fundamentals and performance metrics are reviewed
• ΣΔ ADC concepts and implementation issues are presented for integrated RF transceivers
• Technology evolution drives ADC scaling in nanometer CMOS
  - Faster devices enable higher sample rate
  - Limited SNR due to low $V_{DD}$ remains the dominant challenge for high-resolution converters
  - High-gain, high-speed amplifier design is another critical issue
• Perspectives of ΣΔ ADC design in nm-CMOS are discussed
• ΣΔ ADCs scale better than Nyquist ADCs