– IMS2007 Workshops –

A/D Converters for Wireless Communication in Nanometer CMOS

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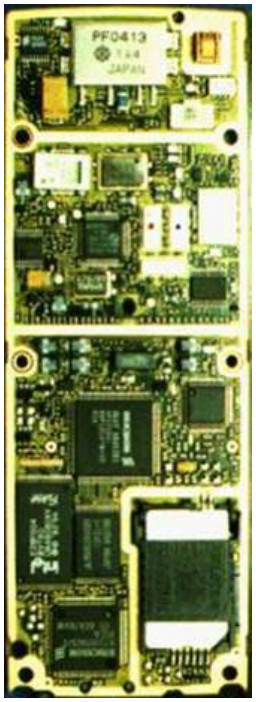
Introduction

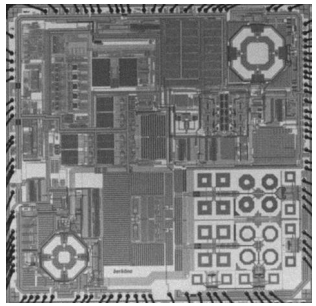
Evolution of RF Transceivers

- **CMOS Technology scaling – Moore's law**
- **Circuit design technique innovations**

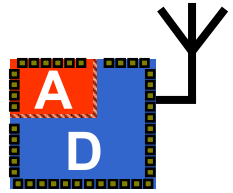


Ericsson CH388
(Hybrid, 1995)

Ericsson Bluetooth
(CMOS, 2001)



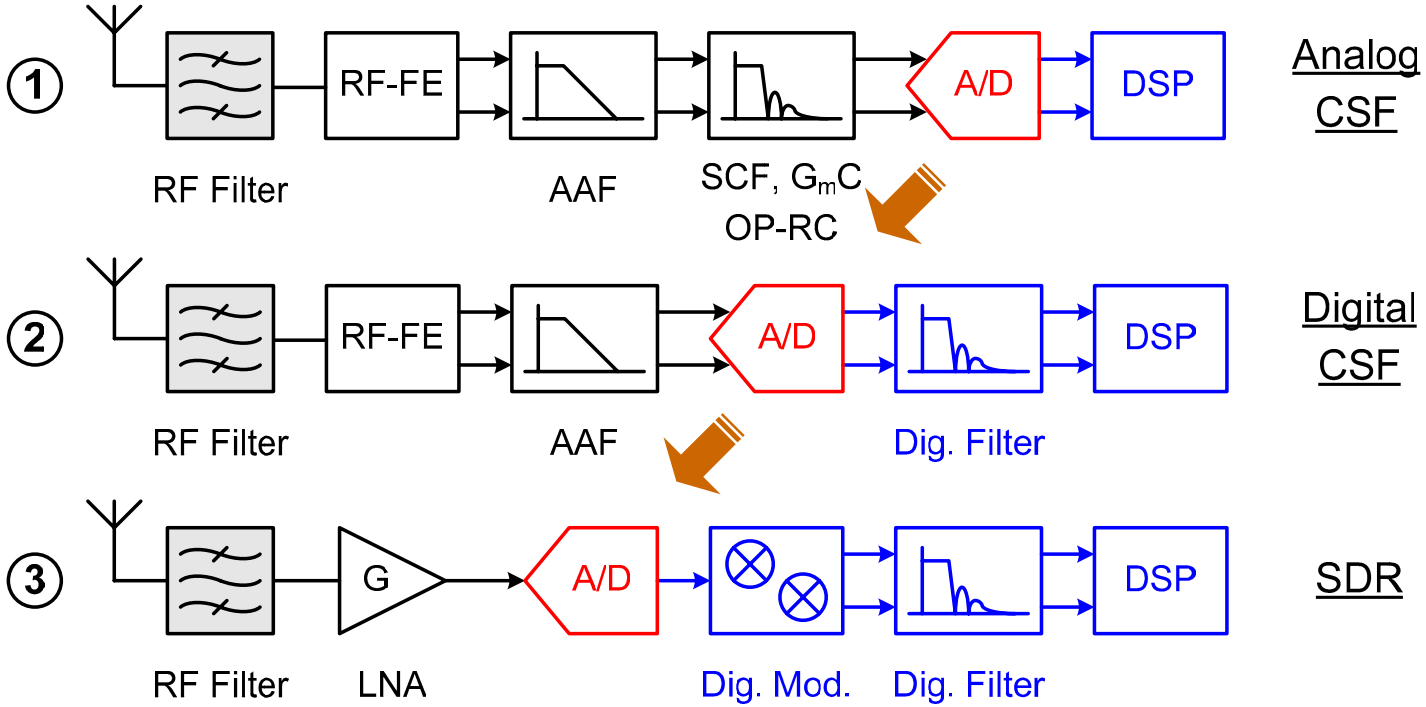
Berkäna GSM/GPRS
(CMOS, 2005)

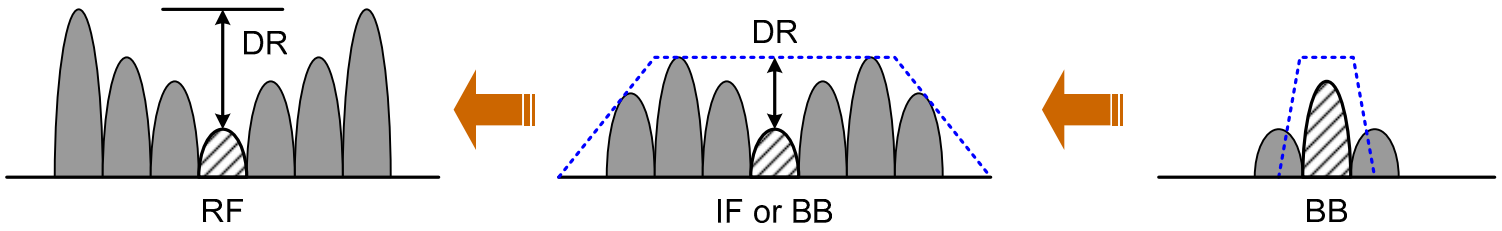


Nano-CMOS?
Nanotube?

Past → **Present** → **Future**

A/D Interface in RF Receivers





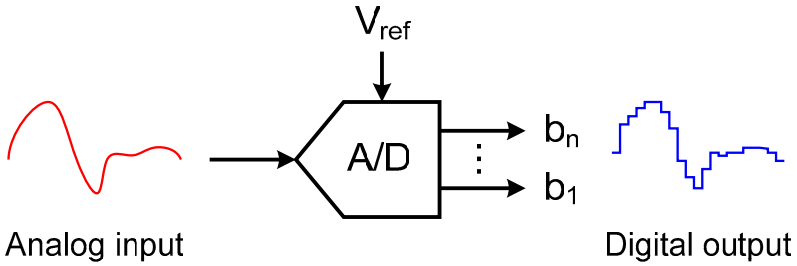
Example: GSM Receiver

Specs	Case 1 (Analog CSF)	Case 2 (Digital CSF)	Case 3 (SDR)
Dynamic Range	20-40 dB	60-80 dB	100 dB
Sample Rate	0.4 MHz	1.6 MHz or 2*IF	2 GHz
Architecture	Nyquist	Sigma-Delta	?
Power	1 mW	10 mW	?
	Trivial	Doable	Outrageous!

- Fundamental tradeoff between linearity (DR) and power consumption
- Judicial system partition results in lowest cost (power, area, technology)
- Power efficiency and linearity are the key concerns for mobile txers

A/D Converter Basics

Signal Quantization

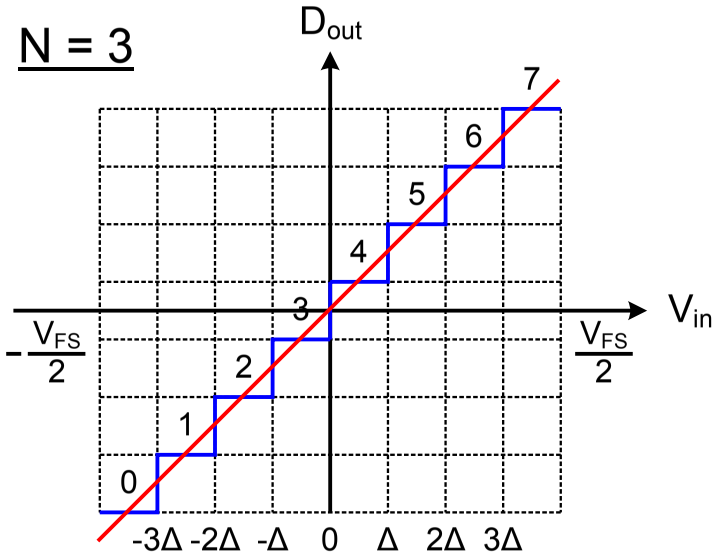


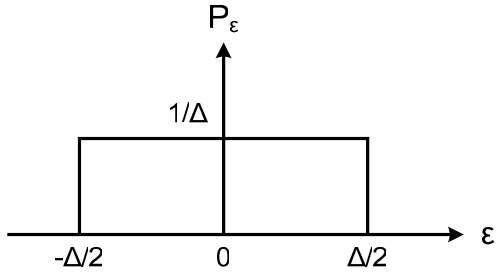
$$\underline{\text{Division}}: \quad D_{out} = \left\lfloor 2^N \cdot \frac{V_{in}}{V_{FS}} \right\rfloor$$

- Quantization = division + normalization + truncation
- Full-scale range (V_{FS}) is determined by V_{ref}

- Static performance metrics
  - Monotonicity
  - Differential nonlinearity (DNL)
  - Integral nonlinearity (INL)
  - Offset
  - Gain error
- Dynamic performance metrics
  - Signal-to-noise ratio (SNR)
  - Signal-to-noise plus distortion ratio (SNDR)
  - Spurious-free dynamic range (SFDR)
  - Aperture uncertainty
  - Dynamic range (DR)
  - Idle channel noise (ΣΔ)

Quantization Error



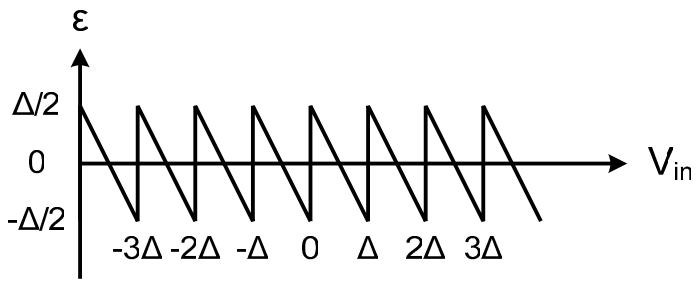


$$-\frac{\Delta}{2} \le \varepsilon \le \frac{\Delta}{2}$$

"Random" quantization error is regarded as noise

$$\sigma_\varepsilon^{\,2} = \int_{-\Delta/2}^{\Delta/2} \varepsilon^2 \cdot \frac{1}{\Delta} \cdot d\varepsilon = \frac{\Delta^2}{12}$$

$$\varepsilon = D_{out}\Delta - V_{in} = D_{out}\left(\frac{V_{FS}}{2^N}\right) - V_{in}$$



Assumptions:

- N is large
- $0 \le V_{in} \le V_{FS}$ and $V_{in} >> \Delta$
- V_{in} is active
- ε is Uniformly distributed
- Spectrum of ε is white

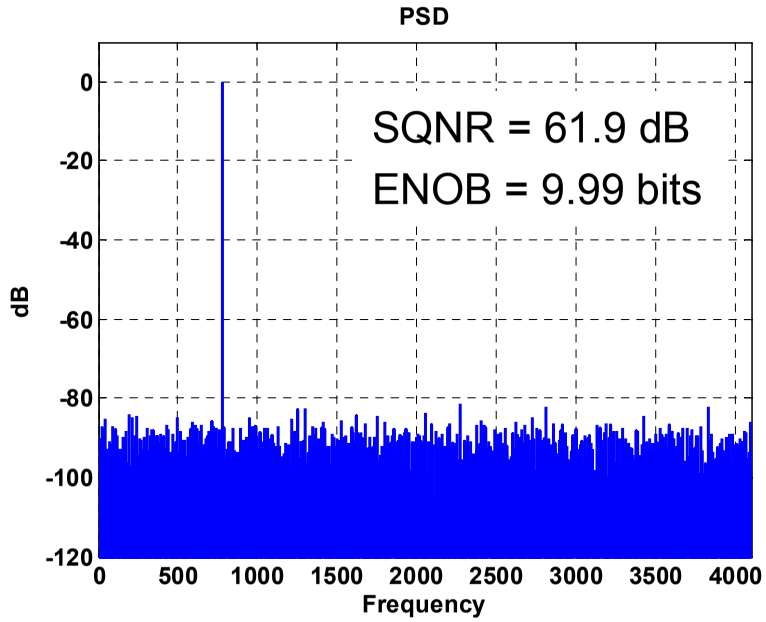
SQNR, ENOB, and QN Spectrum

Assume V_{in} is sinusoidal with $V_{p\text{-}p} = V_{FS}$

$$SQNR = \frac{V_{FS}^{\ 2}/8}{\sigma_{\varepsilon}^{\ 2}} = \frac{\left(2^N \Delta\right)^2/8}{\frac{\Delta^2}{12}} = 1.5 \times 2^{2N}$$

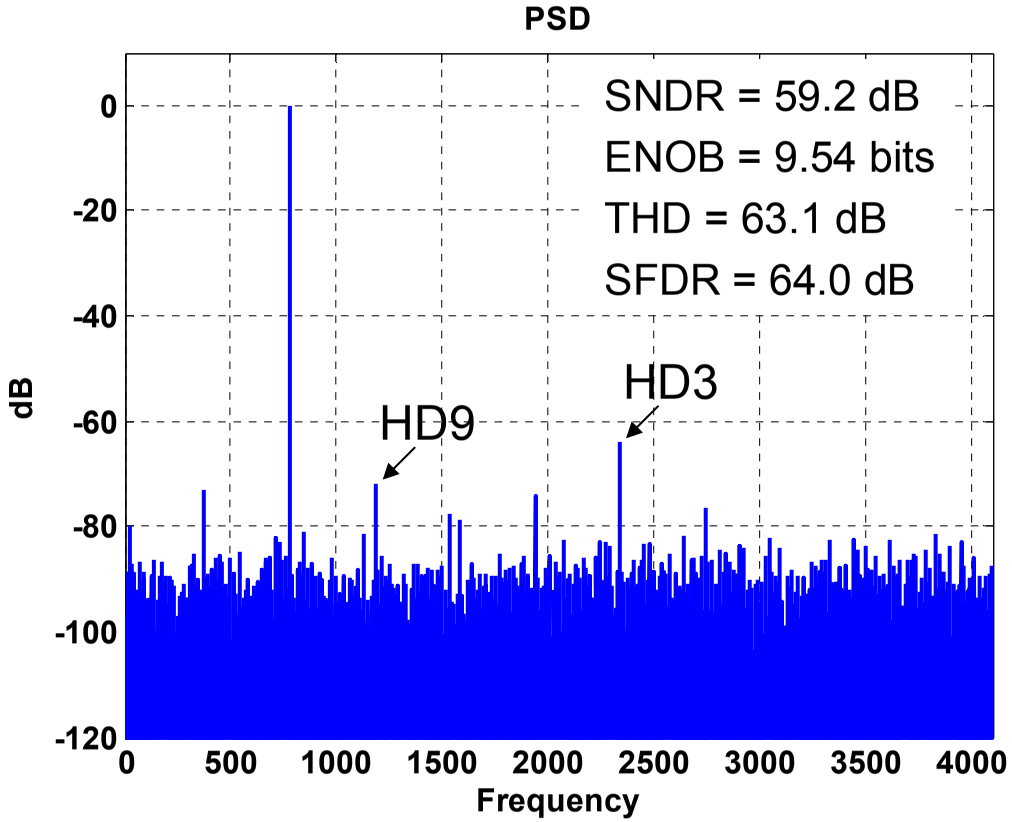
$$\boxed{SQNR = 6.02N + 1.76dB}$$

$$\boxed{ENOB = \frac{SQNR - 1.76}{6.02}}$$



- SQNR depicts the theoretical performance of an ideal ADC
- In reality, ADC performance is limited by many other factors
  - Electronic noise (thermal, 1/*f*, coupling, and etc.)
  - Distortion (measured by THD, SFDR)

Typical Nyquist ADC Output Spectrum

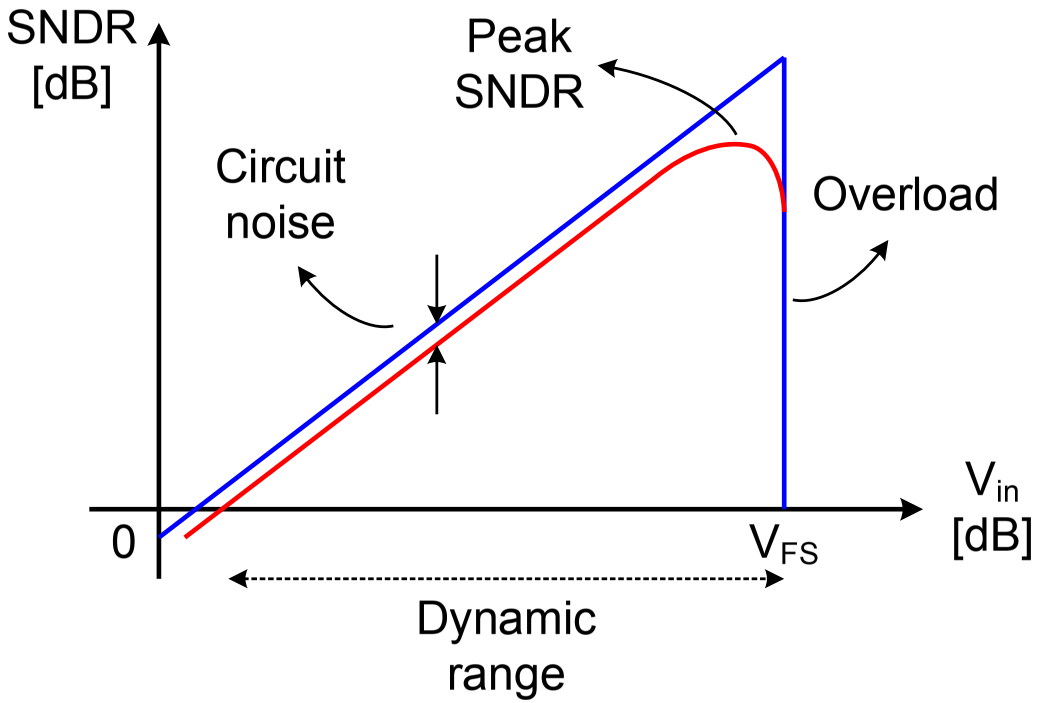


- Signal-to-noise plus distortion ratio (SNDR)
- Total harmonic distortion (THD)
- Spurious-free dynamic range (SFDR)

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02}$$

- High-order harmonics are aliased back, visible in [0, f_s/2] band
- Eg: HD3 @ 779x3+1=2338, HD9 @ 8192-9x779+1=1182

ADC Dynamic Performance

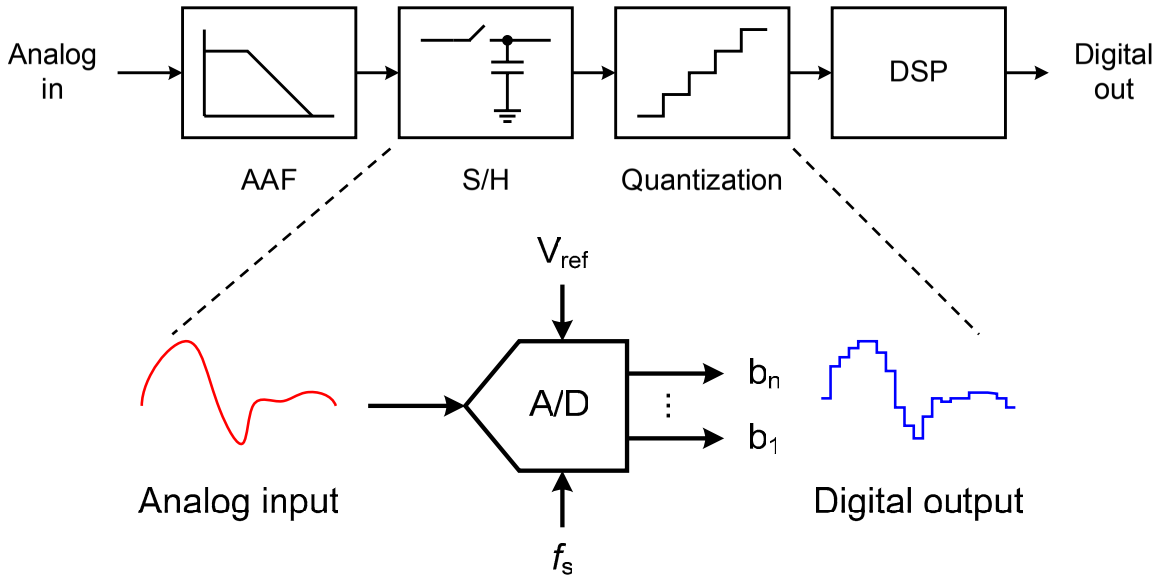


$$SNDR = 10LOG\left(\frac{V_{in}^{2}/2}{\Delta^{2}/12 + \sigma_{N}^{2}}\right)$$
$$\propto 20LOG(V_{in})$$
$$\propto V_{in}(dB)$$

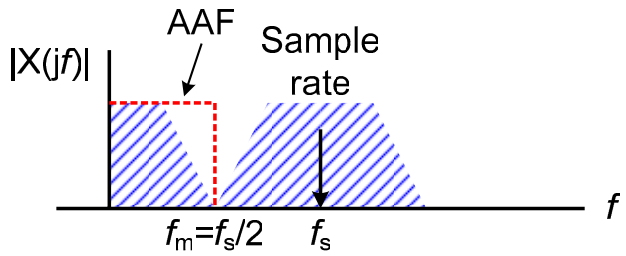
- Peak SNDR limited by large-signal distortion of the converter
- Dynamic range implies the “theoretical” SNR of the converter

Sigma-Delta vs. Nyquist ADCs

Nyquist-Rate ADC



- Sample by sample
- Memoryless
- Minimum sample rate



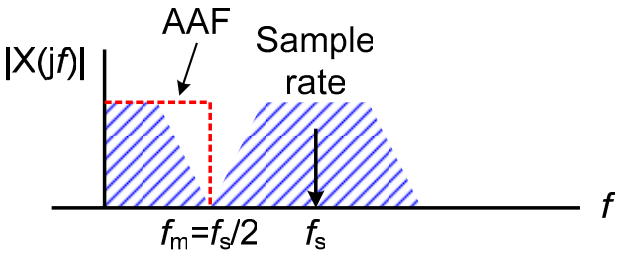
Nyquist-sampling

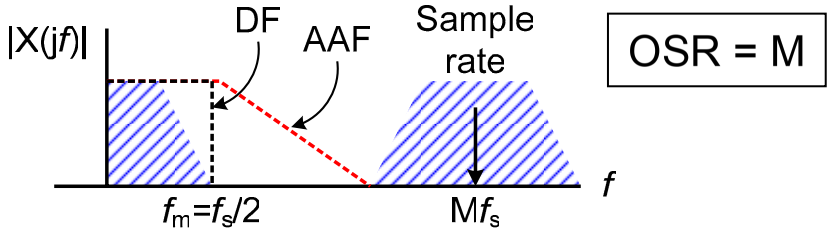
Architecture:

- Word-at-a-time (1 step)†
  - Flash
  - Folding
- Level-at-a-time (2^N steps)†
  - Integration (Serial)
- Bit-at-a-time (N steps)†
  - Successive approximation
  - Algorithmic (Cyclic)
- Partial word-at-a-time ($1<M\leq N$ steps)†
  - Subranging
  - Multi-step
  - Pipeline

† Latency, not throughput

Sigma-Delta (ΣΔ) ADC

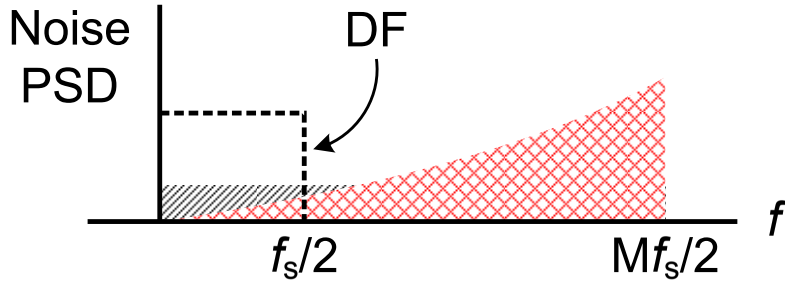


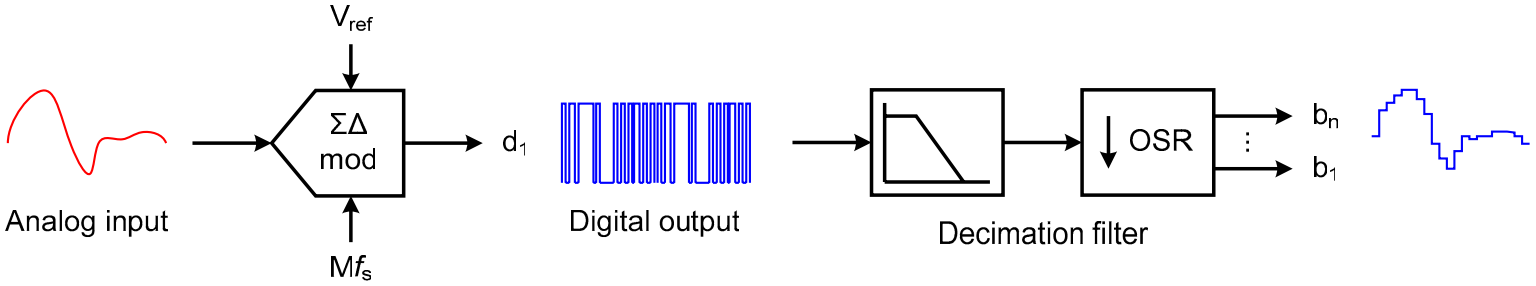


Nyquist-sampling

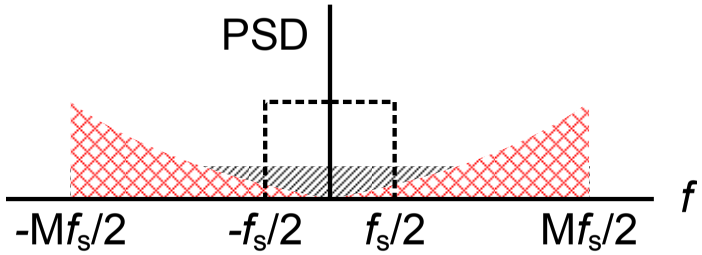
Oversampling: much relaxed AAF

- Oversampling with M >> 1
- **Quantization noise shaping**
- Low-resolution quantization
- Digital decimation filter required

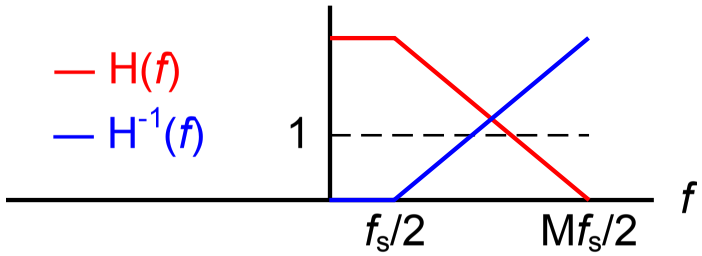




Noise Shaping Basics

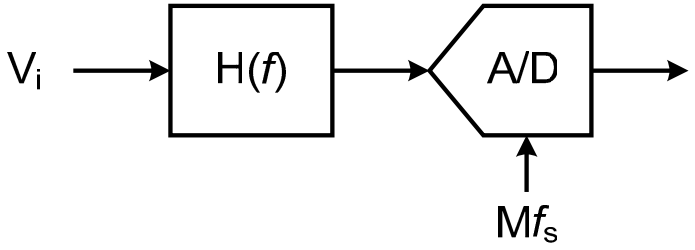


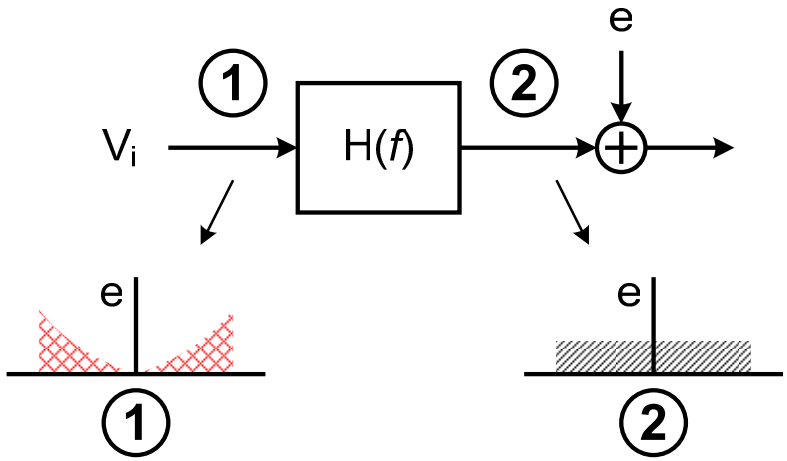
Push noise out of signal band



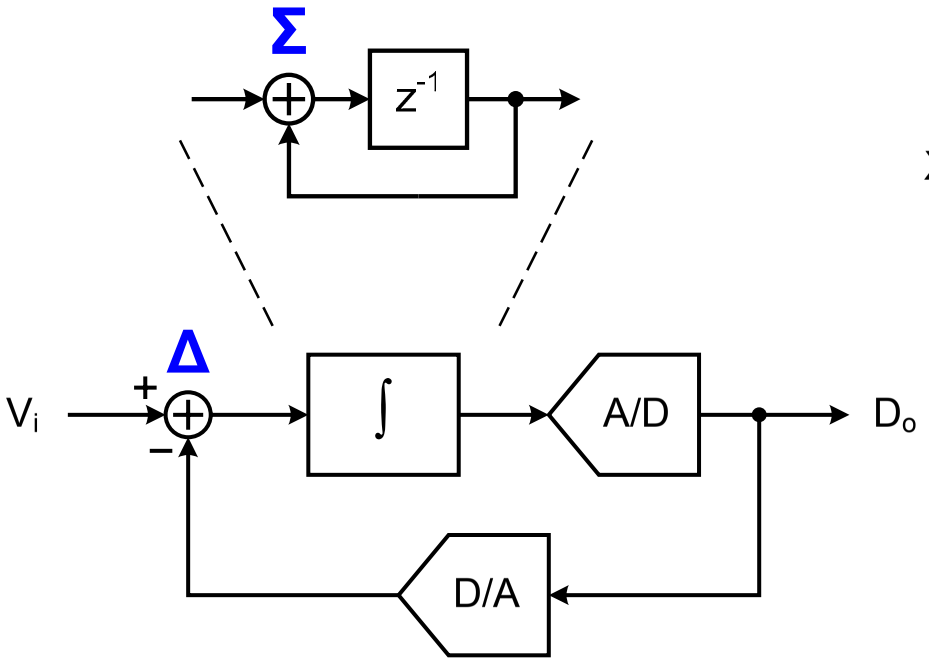
High gain @ LF, low gain @ HF

→ **Integrator**?

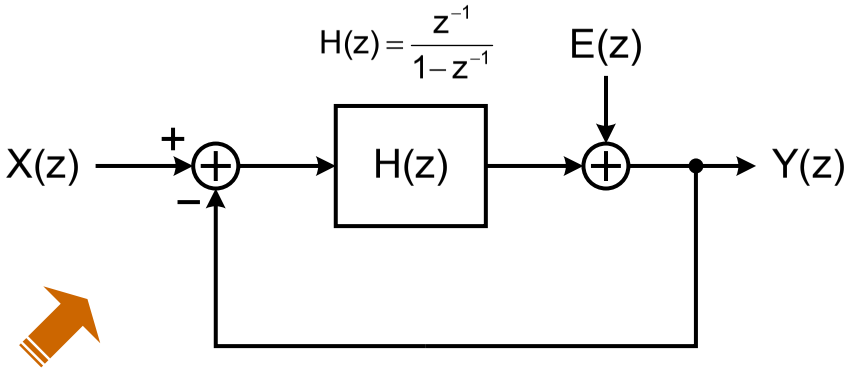




ΣΔ Modulator



1st-order ΣΔ modulator



Linearized z-domain model

$$Y(z) = z^{-1} \cdot X(z) + \left(1 - z^{-1}\right) \cdot E(z)$$

Signal Transfer Function :

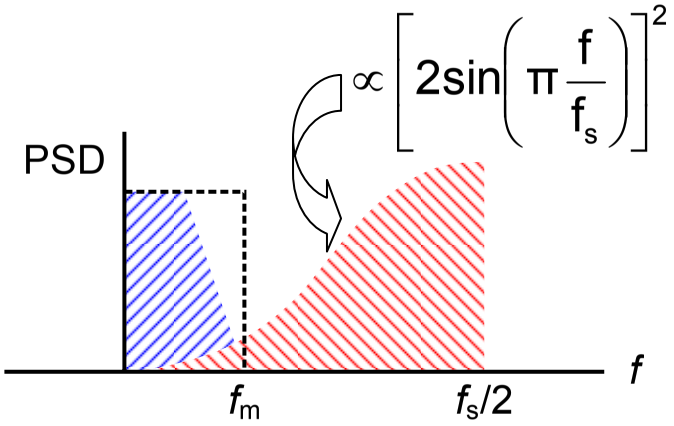
$STF = z^{-1} \leftarrow$ Delay

Noise Transfer Function :

$NTF = 1 - z^{-1} \leftarrow$ HP

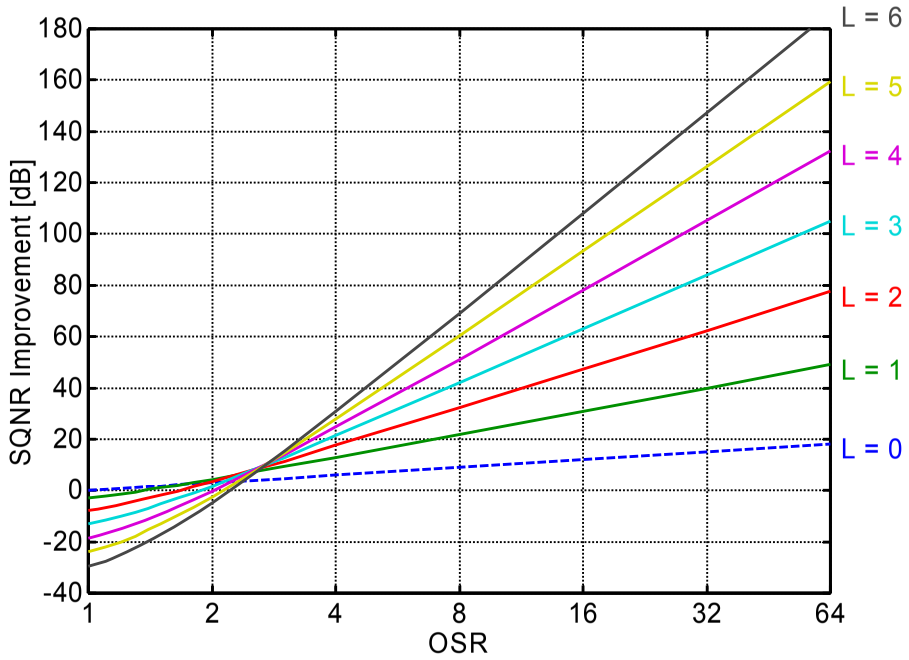
- Integrator performs noise shaping
- D/A feedback to avoid ∫ saturation

Noise Transfer Function



In - band quantization noise :

$$N_e^2 \approx \frac{\Delta^2}{12}\cdot\frac{\pi^2}{3M^3}$$



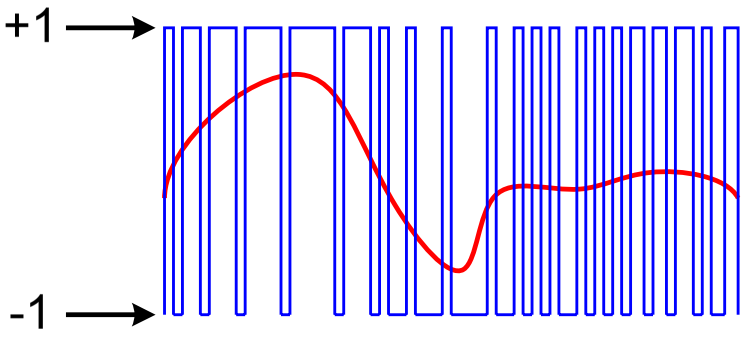
$$Y(z) = z^{-n}X(z) + \left(1 - z^{-1}\right)^L E(z)$$

$$N_e^2 \approx \frac{\Delta^2}{12}\cdot\frac{\pi^{2L}}{(2L+1)\cdot M^{2L+1}}$$

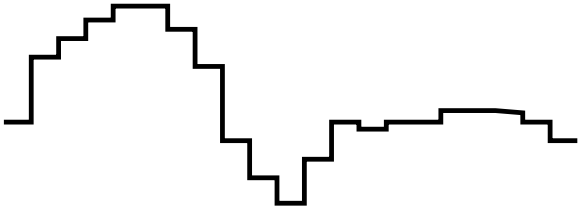
- Doubling OSR (M) increases SQNR by (6L+3) dB, or (L+0.5) bit
- Potential instability for 3rd- and higher-order single-loop ΣΔ modulators

ΣΔ vs. Nyquist ADCs

ΣΔ ADC output (1-bit)



Nyquist ADC output



Nyquist:

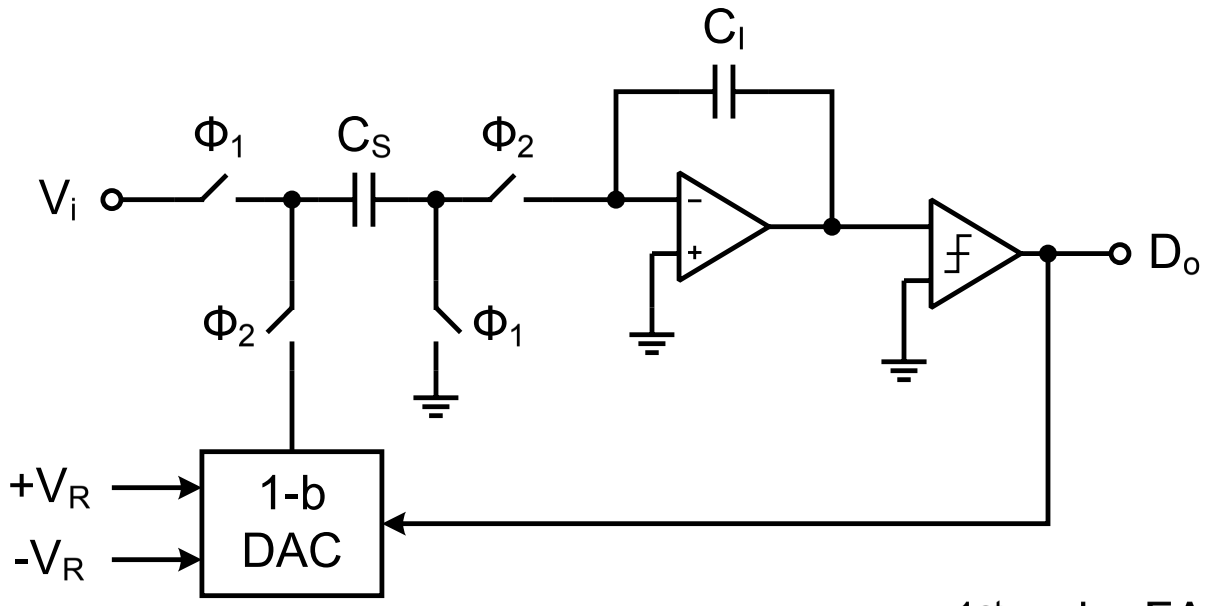
- Sample by sample, memoryless, each sample resolved to N bits

ΣΔ:

- The digital codes only display an “average” impression of the input
- INL, DNL, monotonicity, missing code, and etc. do not directly apply in ΣΔ converters → use SNR, SNDR, SFDR instead (DR not rec’d)

Implementation Aspects of ΣΔ ADC

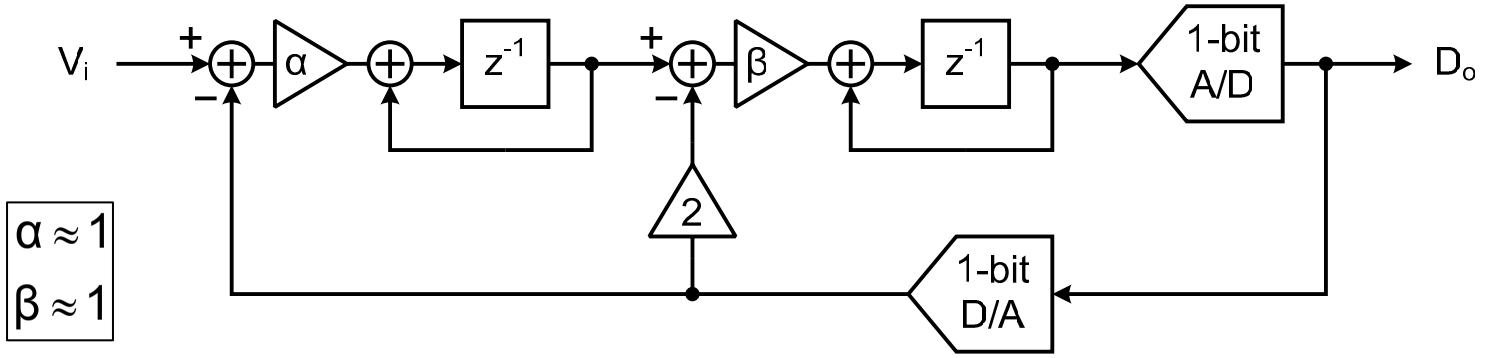
Implementation Simplicity



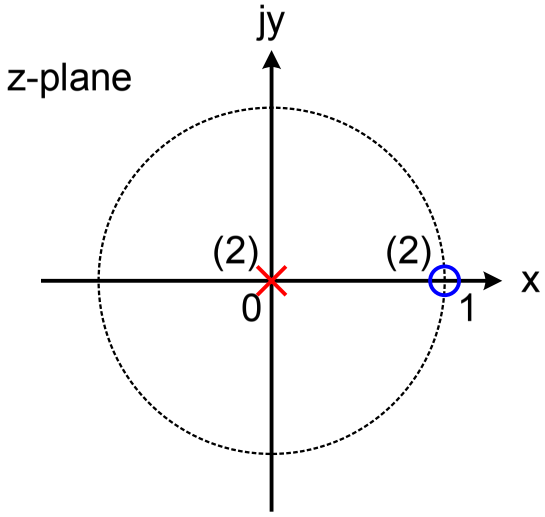
1st-order ΣΔ ADC

- SC integrator, sampling at input
- 1-bit ADC → simple, ZX detector
- 1-bit feedback DAC → simple, inherently linear
- Quantization noise highly correlated with input → “tones”

Insensitive to Component Mismatch

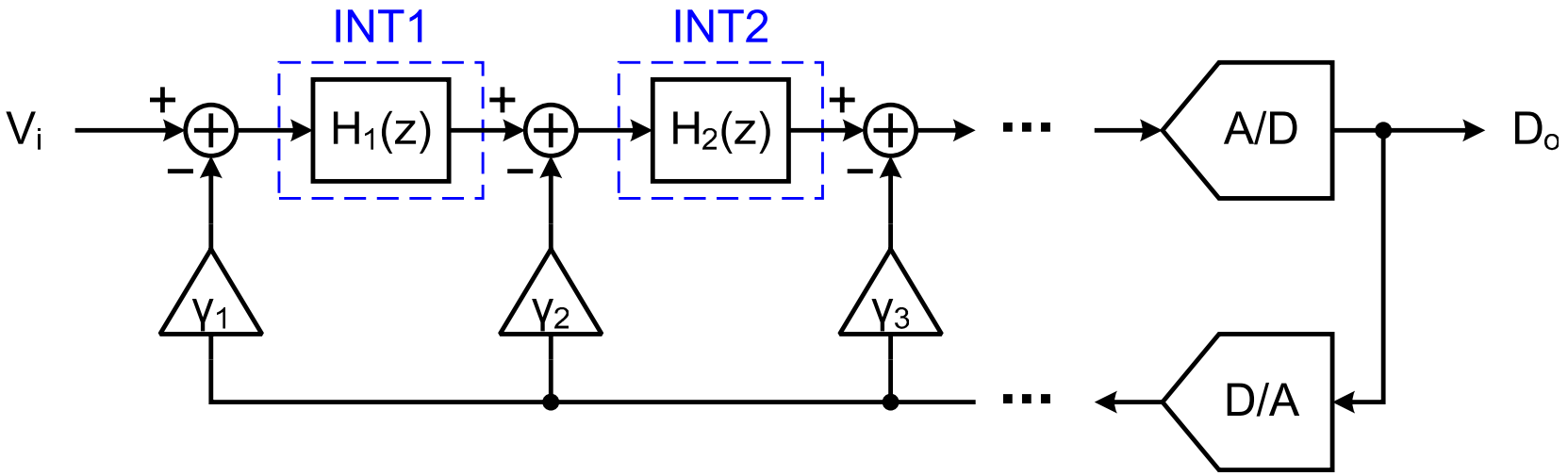


$$D_o(z) = \frac{\alpha}{z^2 + \alpha - 1} V_i(z) + \frac{(z-1)^2}{z^2 + \alpha - 1} E(z)$$



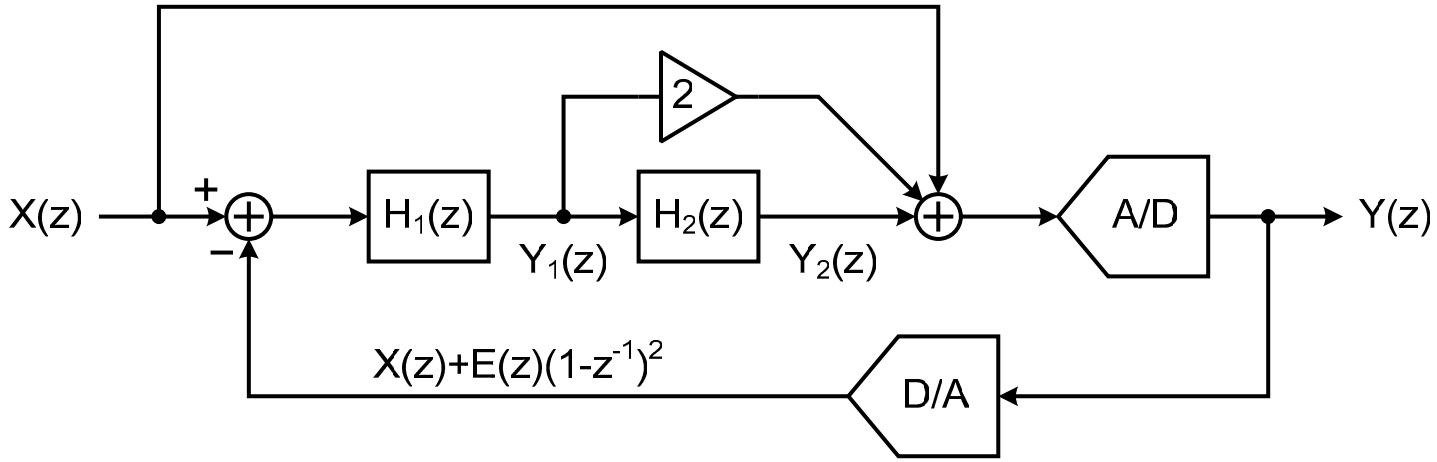
- Less correlation b/t E(z) and $V_i(z)$
- Simple, stable, highly-linear
- **Insensitive to component mismatch**
- **Relaxed op-amp gain requirement**

High-Order Single-loop ΣΔ Modulator



- Higher order noise shaping (L ≥ 3) is obtained
- Relaxed circuit components w/ single-bit quantizer and D/A
- Subject to stability issues for L ≥ 3
- Integrator gains and feedback coefficients need to be carefully optimized to avoid overload; resets each integrator output if occurs

Feedforward Compensation (1)



$$STF = \frac{1 + 2H_1 + H_1H_2}{1 + 2H_1 + H_1H_2} = 1$$

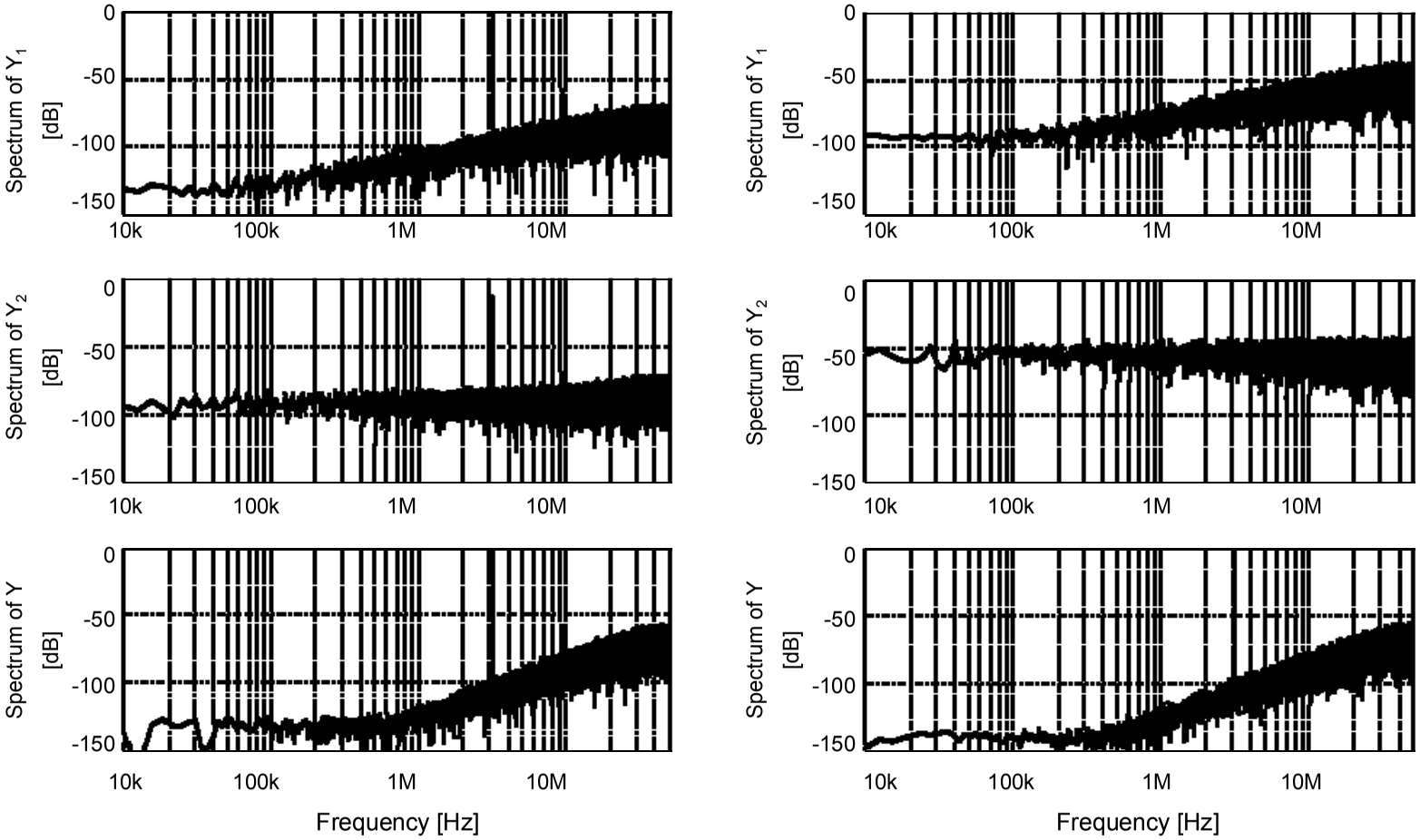
$$NTF = \frac{1}{1 + 2H_1 + H_1H_2} = \left(1 - z^{-1}\right)^2$$

- Eliminates circulating signal in the loop → less likely to be unstable
- Only quantization noise processed by the integrators
- Less signal swing at integrator outputs → less op-amp swing required and less distortion → good for low V_{DD} implementation

Feedforward Compensation (2)

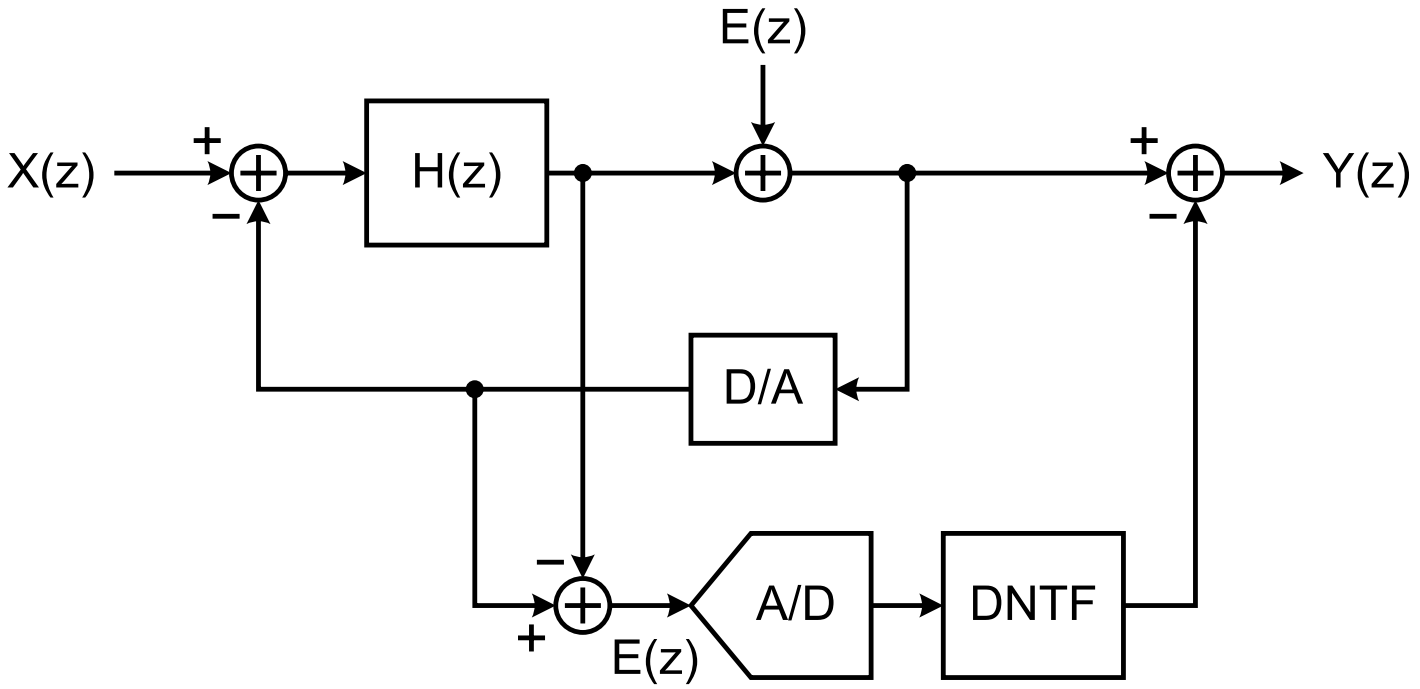
MATLAB simulations w/ nonlinear function included in 1st integrator

w/o feedforward† | w/ feedforward†



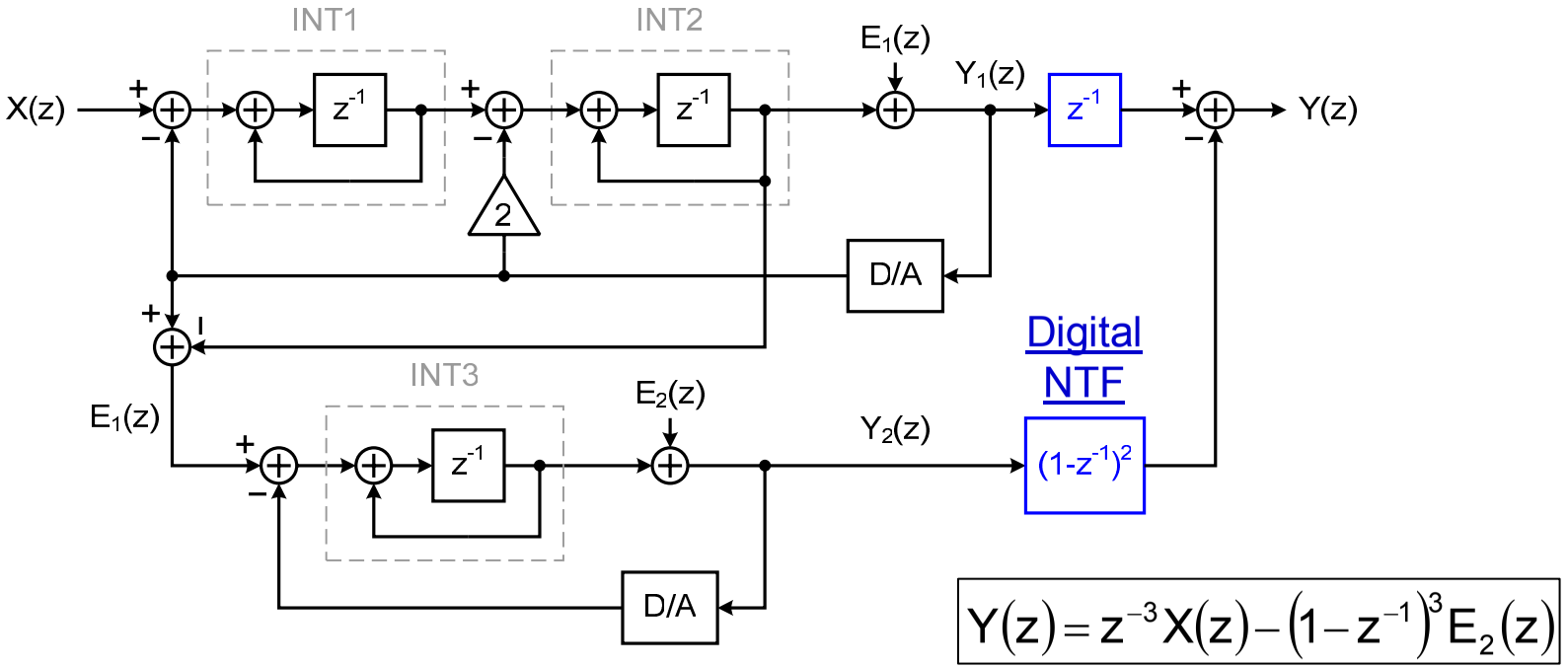
† Courtesy of Prof. Gabor Temes, OSU

The Cascaded Architecture (MASH)



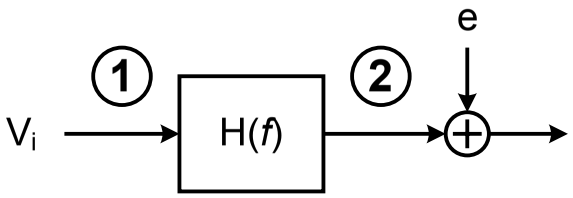
- Idea: to further quantize E(z) and later subtracted in digital domain
- The basic modulator is limited to 2nd order → not subject to instability
- The 2nd quantizer is typically a ΣΔ modulator as well

MASH 2-1 Cascaded Modulator

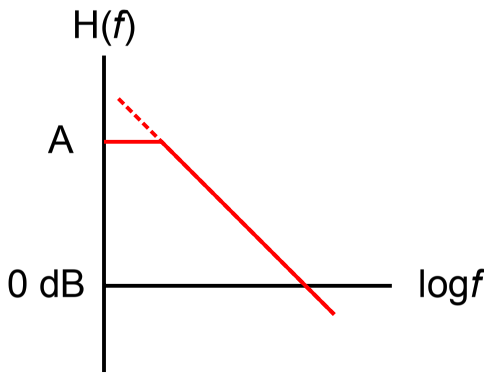


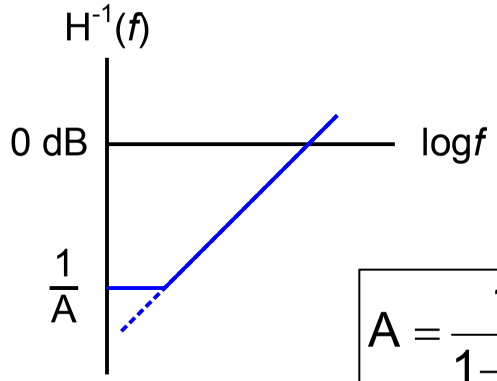
- $E_1(z)$ completely cancelled assuming perfect matching between the modulator NTF (analog domain) and the DNTF (digital domain)
- A 3rd-order noise shaping on $E_2(z)$ obtained w/o stability issues
- Caveat: sensitive to mismatch (analog NTF ≠ digital NTF)

Integrator "Leakage"

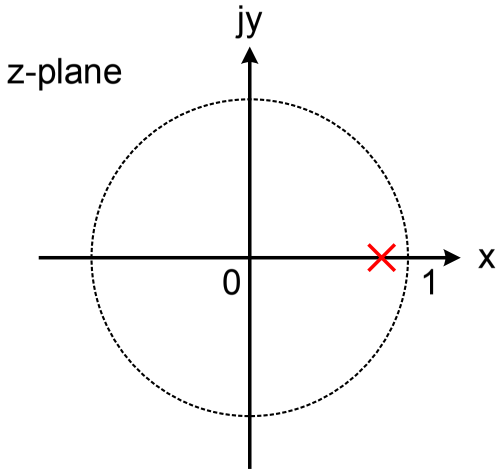


$$H(z) = \frac{z^{-1}}{1-\alpha z^{-1}}, \quad \alpha < 1$$



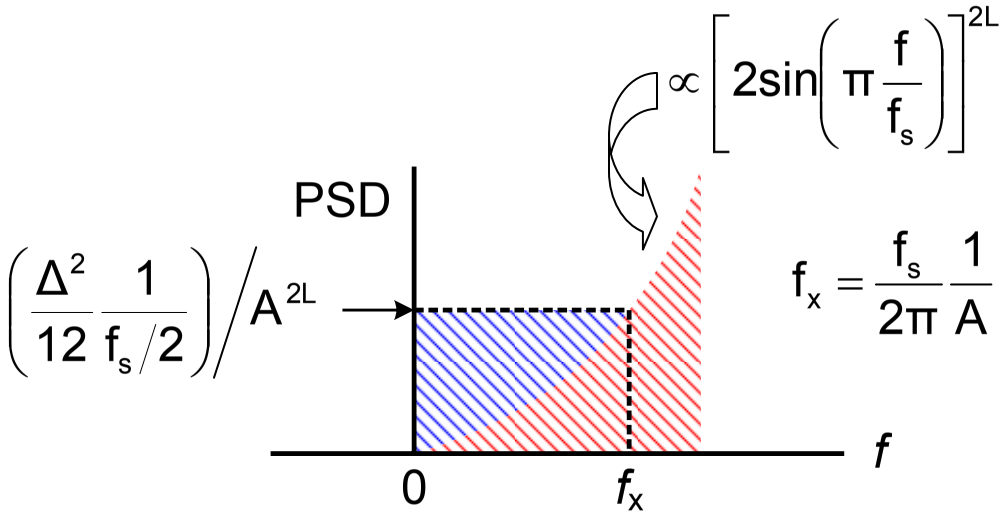


$$A = \frac{1}{1-\alpha}$$



- Finite op-amp gain introduces noise leakage into the signal band
- Leakage can also result in "dead zone" for small input voltages

How Much Gain Is Enough?



Set $A_{BLUE} = N_e^2$

(3dB loss in SQNR)

$$A = \frac{M}{\pi}\sqrt[2L+1]{2L} \approx \frac{M}{\pi}$$

$$A_{RED} = \int_0^{f_x} \frac{\Delta^2}{12}\cdot\frac{1}{f_s/2}\cdot|NTF|^2 df \approx \frac{\Delta^2}{12}\cdot\frac{1}{\pi(2L+1)}\cdot\frac{1}{A^{2L+1}}$$

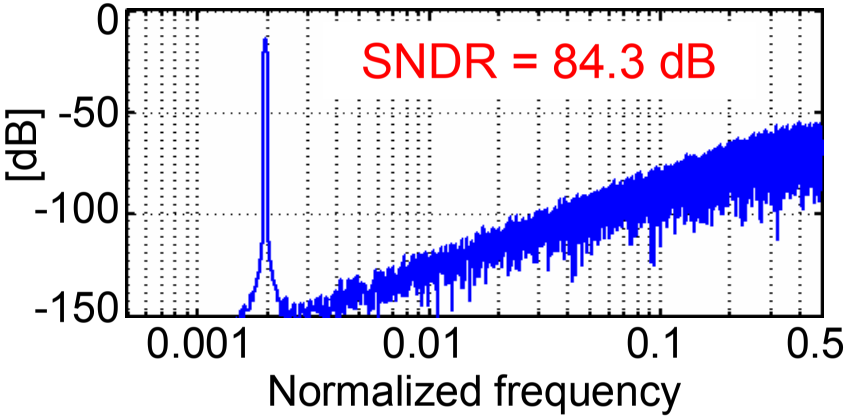
$$A_{BLUE} = f_x\left(\frac{\Delta^2}{12}\cdot\frac{1}{f_s/2}\right)\Big/A^{2L} - A_{RED} \approx \frac{\Delta^2}{12}\cdot\frac{2L}{2L+1}\cdot\frac{1}{\pi A^{2L+1}}$$

- Input-referred circuit noise of the 1st integrator dominates over QN
- Actual required op-amp gain is determined by distortion specs

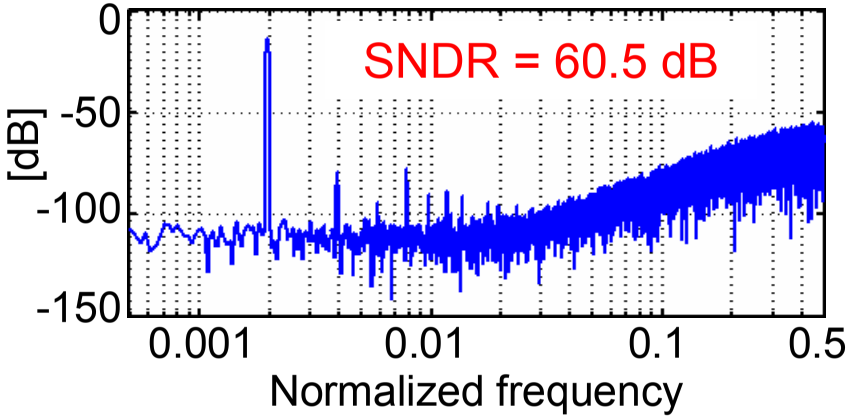
DAC Nonlinearity

2nd-order ΣΔ Modulator (4-b A/D and D/A), OSR = 32, ideal SNDR ≈ 14 b

Ideal DAC†



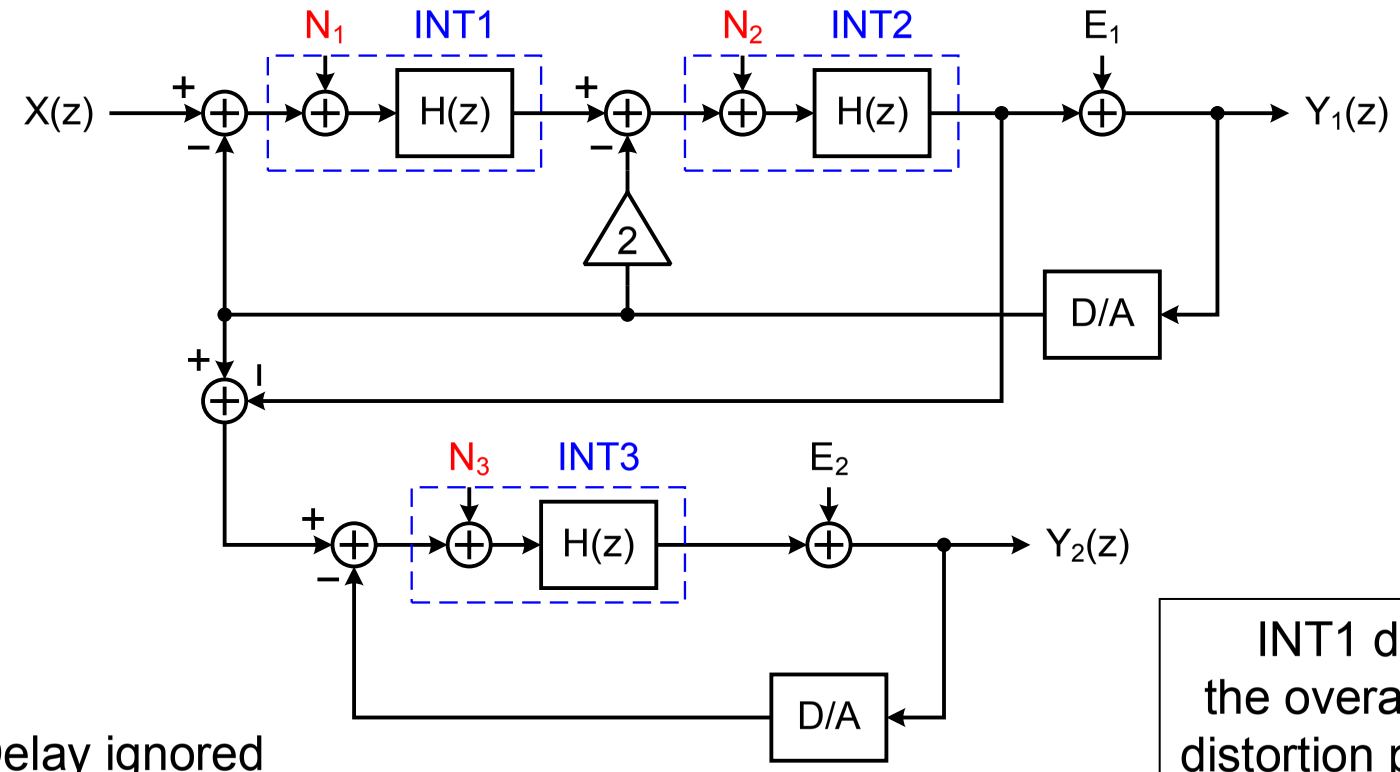
10-bit linear DAC†



- 2-level SE or 3-level DF DAC can be made perfectly linear
- Multi-bit DAC nonlinearity directly adds to the summing node, limiting the ΣΔ Modulator linearity and quantization noise performance
- In general, linearity of ΣΔ Modulator is no better than that of the DAC – use mismatch-shaping DAC or DEM/DWA

† Courtesy of Prof. Gabor Temes, OSU

Integrator Noise and Distortion



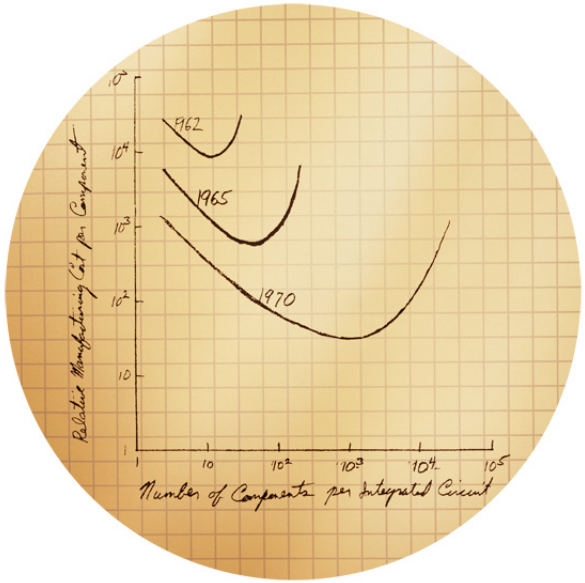
Delay ignored

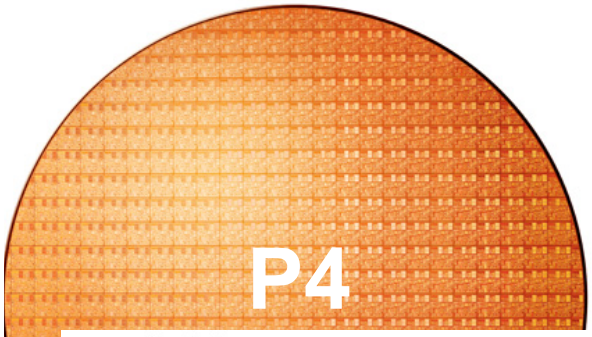
INT1 dominates the overall noise and distortion performance!

$$Y = X + N_1 + (1 - z^{-1})N_2 + (1 - z^{-1})^2 N_3 + \delta(1 - z^{-1})^2 E_1 + (1 - z^{-1})^3 E_2$$

Technology Scaling and Impact on ΣΔ ADC

Technology Scaling Trend



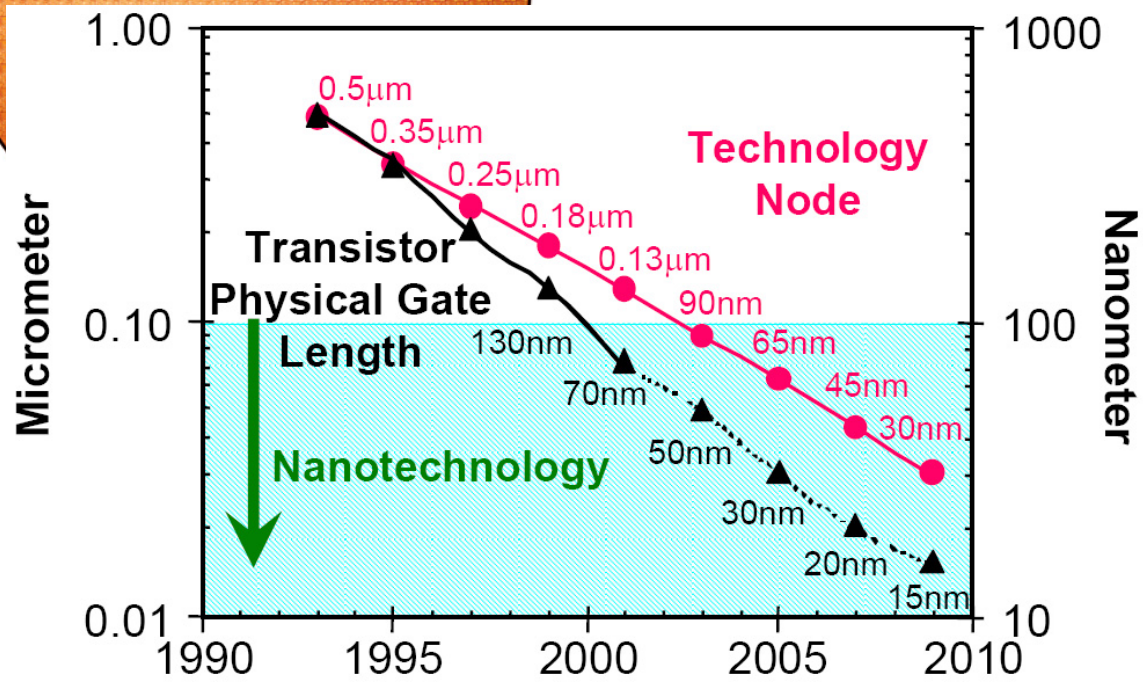


R. Chau, *ICSICT* '04

"The number of transistors on a chip doubles every 18 months…"

- Gordon Moore, *IEDM* 1975

Source: *www.intel.com*



ΣΔ ADC Design in nm-CMOS

Technology scaling offers:

- High f_T
- Low V_{DD}
- Elevated device noise
- Low intrinsic gain ($g_m \cdot r_{out}$)
- Sub-threshold/gate leakage
- Better matching [Pelgrom98]

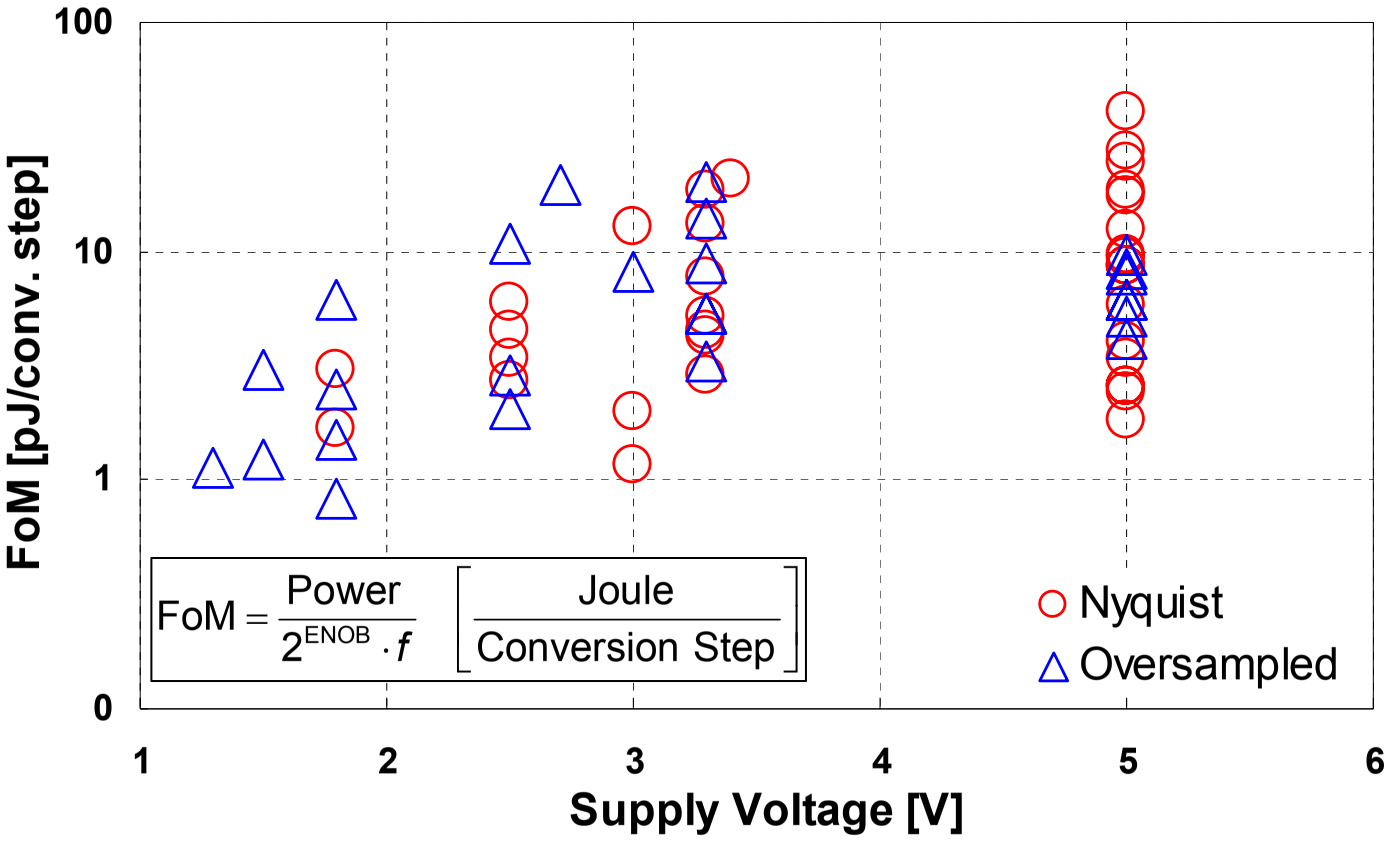
ΣΔ ADC Design perspective:

- Faster amplifier → large M
- Difficult to achieve high ENOB → high power?
- High-gain amplifier?
- Switched-capacitor?
- Determined by size

- Large OSR enables wideband applications
- Noise shaping helps to reduce later stage power/area
- Decimation filter, DWA, digital correction/calibration scale well

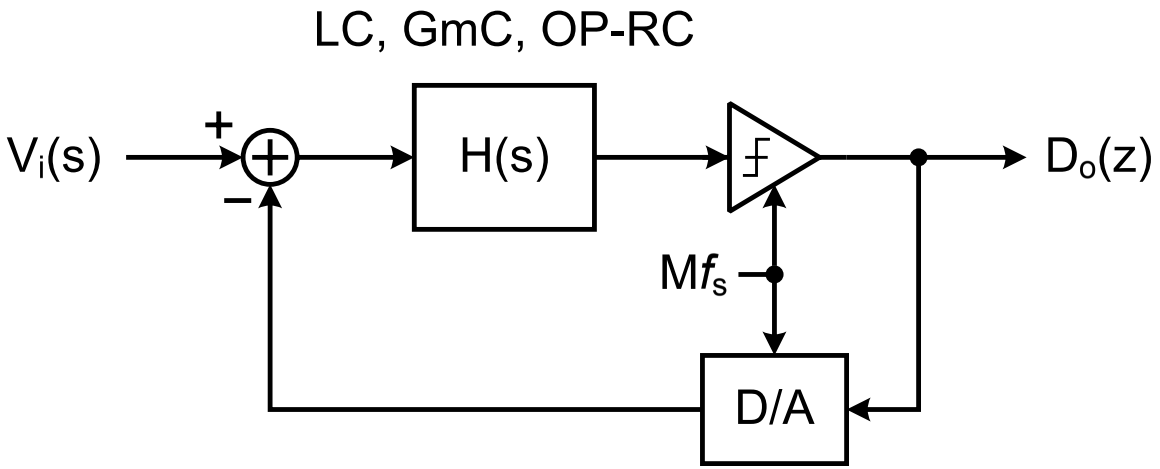
ADC FoM Scaling (≥12 bits)

ΣΔ ADCs scale better than Nyquist ADCs!



Sources: *JSSC*, *ISSCC*, *CICC*, *VLSI*, *ESSCIRC*

CT ΣΔ ADC for Wireless Communication

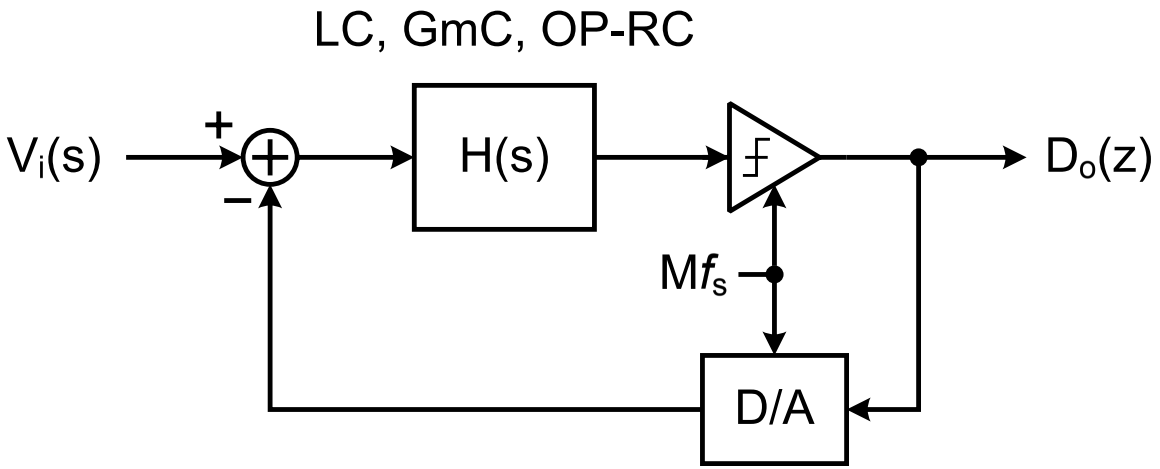


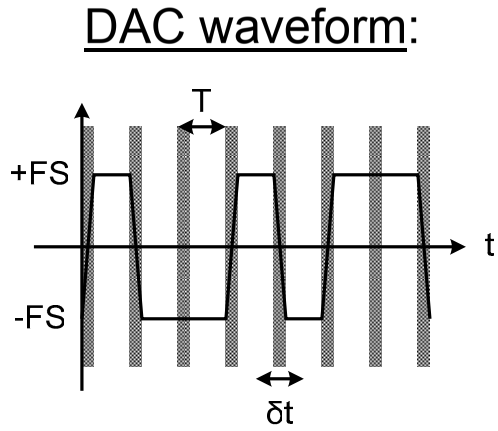
Resonator:

$$H(s) = \frac{\omega_0 s}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^{\,2}}$$

- Integrator is replaced by CT resonator (also functions as AAF)
- Sampling is performed within the loop, not at very input
- Comparator and DAC (switched current) still work in discrete time
- Viable alternative to SC in nm-CMOS with leaky switches

Challenges for CT ΣΔ ADC





- Large op-amp gain and BW required to make summing node ideal
- Integration is performed over the entire clock period of DAC – needs return-to-zero (RZ) pulse shaping to maintain constant pulse width
- Sensitive to DAC clock jitter – use multi-bit A/D, alternative D/A pulse
- Typically requires frequency tuning on H(s) which is analog

Summary

- ADC fundamentals and performance metrics are reviewed
- ΣΔ ADC concepts and implementation issues are presented for integrated RF transceivers
- Technology evolution drives ADC scaling in nanometer CMOS
  - Faster devices enable higher sample rate
  - Limited SNR due to low V_{DD} remains the dominant challenge for high-resolution converters
  - High-gain, high-speed amplifier design is another critical issue
- Perspectives of ΣΔ ADC design in nm-CMOS are discussed
- ΣΔ ADCs scale better than Nyquist ADCs